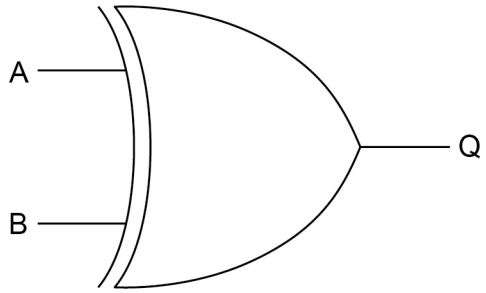
0 1 . 1 **Figure 1** shows a logic gate symbol.

Write the name of the logic gate underneath the figure.

[1 mark]

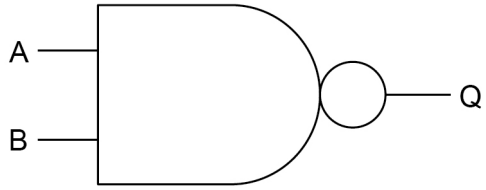
Figure 1



Answer: _____

0 1 . 2 **Figure 2** shows a logic gate symbol.

Figure 2



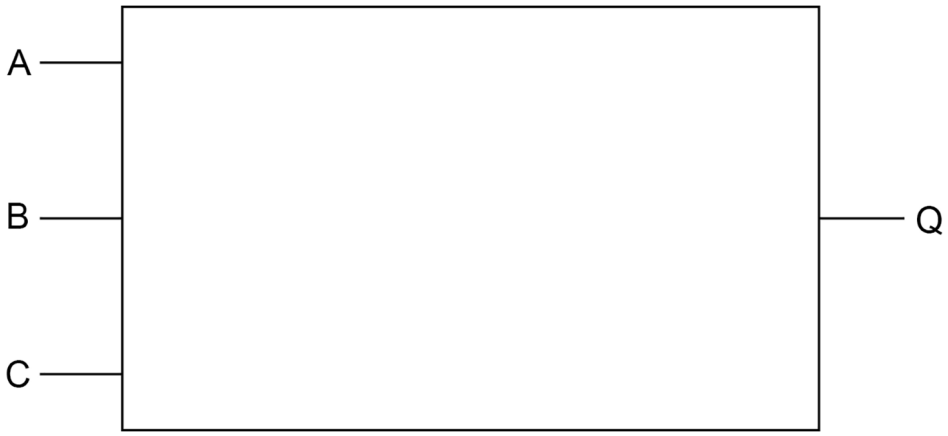
Complete the truth table below for the logic gate shown in **Figure 2.**

[1 mark]

A	B	Q
0	0	
0	1	
1	0	
1	1	

0 1 . 3 Represent the Boolean equation $\overline{A} + \overline{B} \cdot C$ as a logic circuit by drawing a diagram of it in the space below.

[3 marks]



0 2 . 1 State the name of the logic gate represented by the truth table shown in **Figure 1**.

[1 mark]

Figure 1

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

Answer: _____

0 2 . 2 A factory has a machine for filling bottles on a conveyor belt.

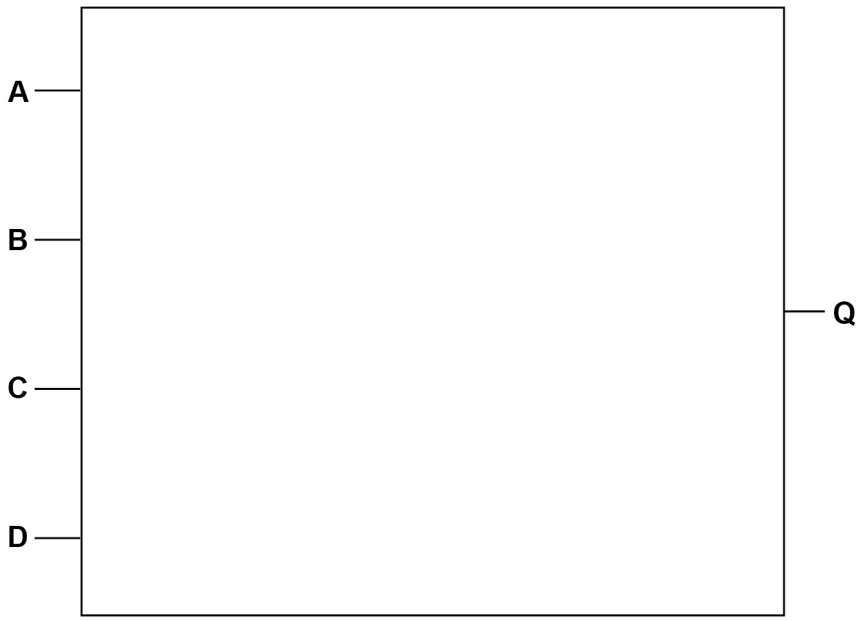
- Q represents the signal to move the conveyor belt on. When Q is set to true the belt will move on.
- A is a sensor which outputs true if a bottle is present.
- B is a sensor which outputs true if a bottle is full.
- C is a sensor which outputs true if a bottle is correctly positioned.
- D is a sensor which outputs true if the next section has a bottle in it.

The conveyor belt is able to move if both of these conditions are true:

- a bottle is full and correctly positioned or there is no bottle present
- there is no bottle in the next section.

In the box below, draw a logic circuit for the machine.

[3 marks]



0 2 . 3 De Morgan's laws can be applied to enable a combination of logic gates to be replaced by a single gate that produces the same output.

What single gate could replace the combination of gates in the expression $\overline{\overline{A} \cdot \overline{B}}$?

[1 mark

0 3 . 1 Complete the truth table for A NAND B.

[1 mark]

A	B	A NAND B
0	0	
0	1	
1	0	
1	1	

0 3 . 2 A XOR B can be implemented as a logic circuit without using an XOR gate.

Using **only** AND, OR and NOT gates draw a circuit that will produce an output **Q** which is logically equivalent to **A XOR B**.

[3 marks]

0 4 . 1 State which logic gate has the truth table shown in **Figure 4**.

[1 mark]

Figure 4

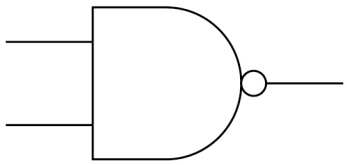
A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

Answer _____

0 4 . 2 State the logic gate that is represented by the symbol shown in **Figure 5**.

[1 mark]

Figure 5

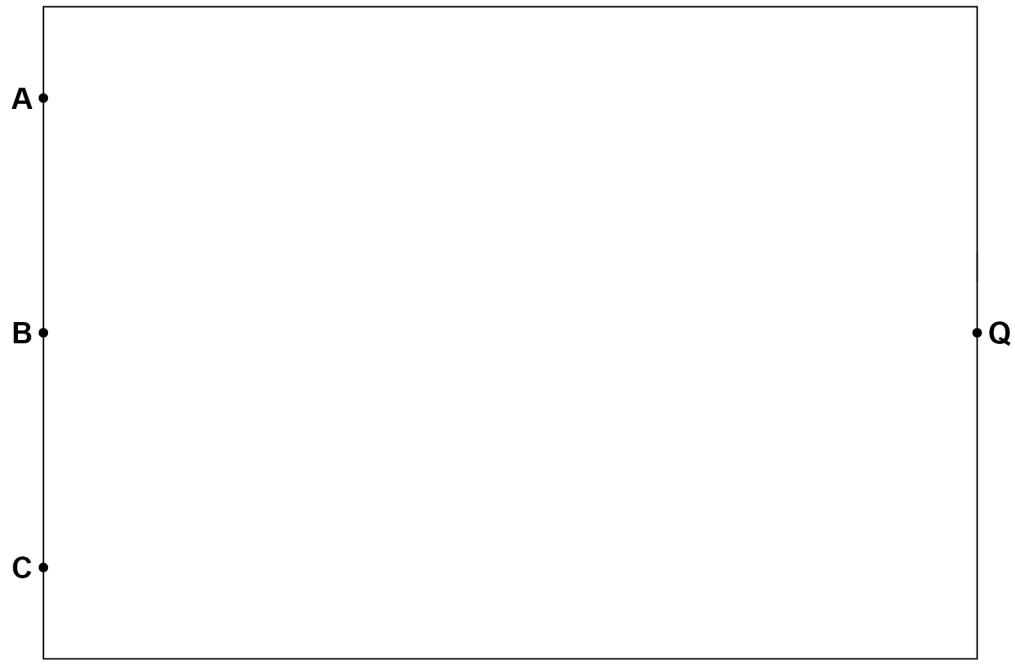


Answer _____

0 4 . 3 Draw the logic circuit for the following Boolean expression.

$$Q = \overline{\overline{A \cdot \overline{B}} + C}$$

[2 marks]



0 4 . 4 Complete the truth table below.

A	B	$\overline{B}$	$(A + \overline{B})$	$(A + \overline{B}) \cdot B$
0	0			
0	1			
1	0			
1	1			

Using the final column, give a simplified Boolean expression for

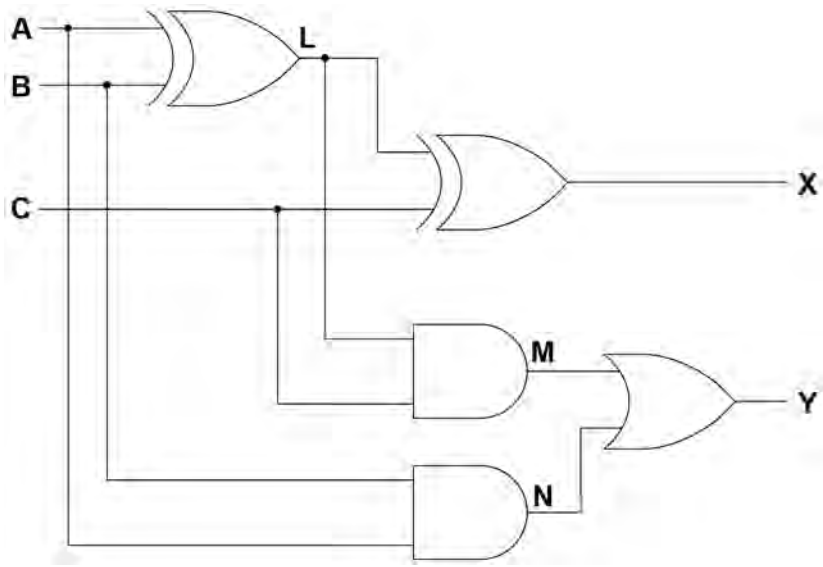
$$(A + \overline{B}) \cdot B$$

[3 marks]

Answer _____

0 5 . 1 **Figure 3** shows a circuit diagram.

Figure 3



Complete the truth table below for the circuit shown in **Figure 3**.

[3 marks]

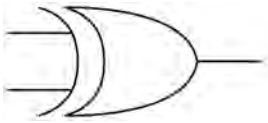
A	B	C	L	M	N	X	Y
0	0	0		0		0	
0	0	1		0		1	
0	1	0		0		1	
0	1	1		1		0	
1	0	0		0		1	
1	0	1		1		0	
1	1	0		0		0	
1	1	1		0		1	

0 5 . 2 Using **Figure 3**, write a Boolean expression for output **Y** in terms of inputs **A**, **B** and **C**.
[2 marks]

Y = _____

0 6 . 1 **Figure 2** shows the symbol for a logic gate.

Figure 2

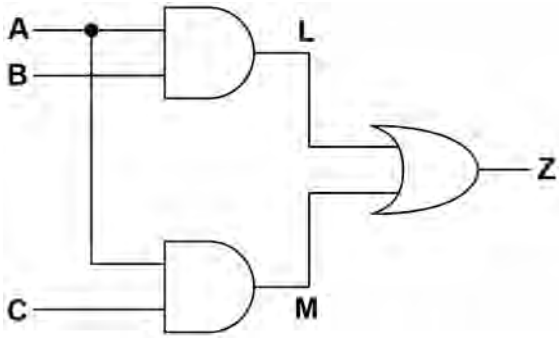


State the name of the logic gate shown in **Figure 2**.

[1 mark]

0 6 . 2 **Figure 3** shows a logic circuit.

Figure 3



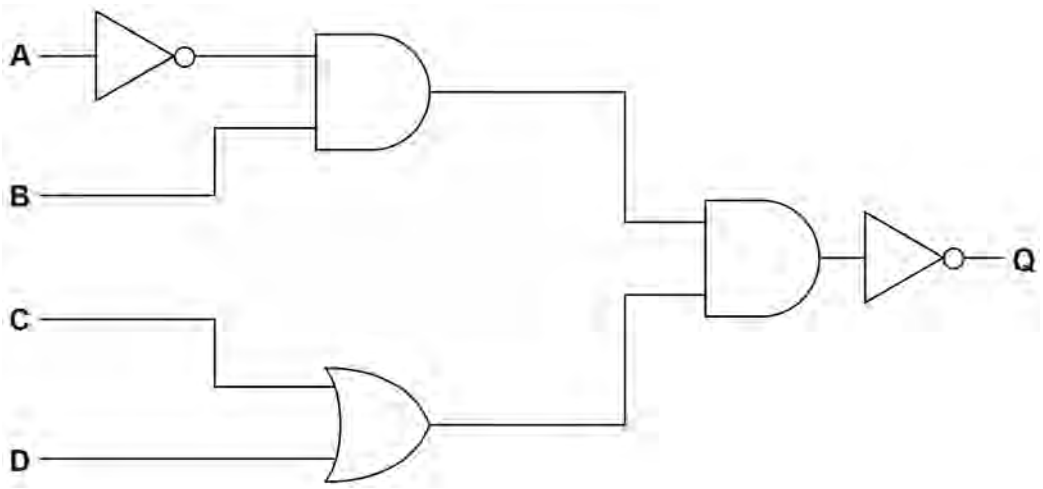
Complete the truth table for the logic circuit in **Figure 3**.

[2 marks]

A	B	C	L	M	Z
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

0 6 . 3 **Figure 4** shows a logic circuit.

Figure 4



Write a Boolean expression for **Q**.

[3 marks]

0 6 . 4 Using the rules of Boolean algebra, simplify the following expression.

$$\overline{W} \cdot X \cdot Z + W \cdot Z + X \cdot Y \cdot \overline{Z} + \overline{W} \cdot X \cdot Y \cdot 1$$

You **must** show your working.

[4 marks]

Final answer _____

0 7 . 1 Complete the truth tables for the OR and NAND gates.

[1 mark]

OR Gate

Inputs		Output
0	0	
0	1	
1	0	
1	1	

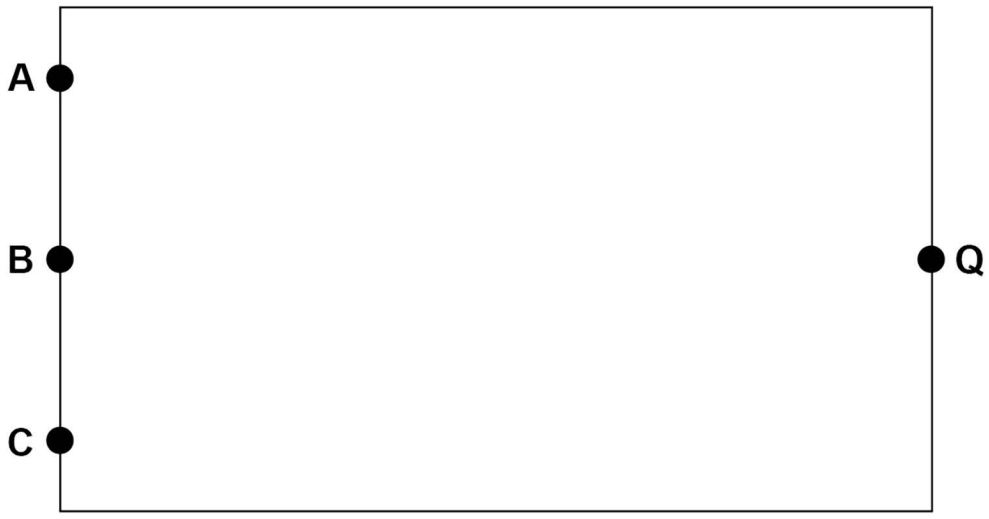
NAND Gate

Inputs		Output
0	0	
0	1	
1	0	
1	1	

0 7 . 2 Draw a logic circuit for the Boolean expression:

$$Q = \overline{A.B + C.\overline{B}}$$

[4 marks]



0 8 . 1 **Figure 6** shows truth tables for four logic gates. The truth tables are labelled **Table A**, **Table B**, **Table C** and **Table D**.

Figure 6

Table A		
Inputs		**Output**
0	0	1
0	1	0
1	0	0
1	1	0

Table B		
Inputs		**Output**
0	0	0
0	1	1
1	0	1
1	1	0

Table C		
Inputs		**Output**
0	0	1
0	1	0
1	0	0
1	1	1

Table D		
Inputs		**Output**
0	0	0
0	1	1
1	0	1
1	1	1

Shade in **one** lozenge to indicate which truth table **does not** represent one of the logic gates: OR, XOR, NOR.

[1 mark]

Table A ⬭

Table B ⬭

Table C ⬭

Table D ⬭

A 7-segment display is a component used to display a digit on devices such as calculators. A 7-segment display consists of seven lights (called segments) which can be illuminated individually to make the shapes of digits. For example, the digit 3 could be displayed by illuminating five of the seven segments like this (black shading indicates an illuminated segment):

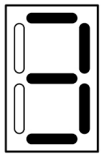
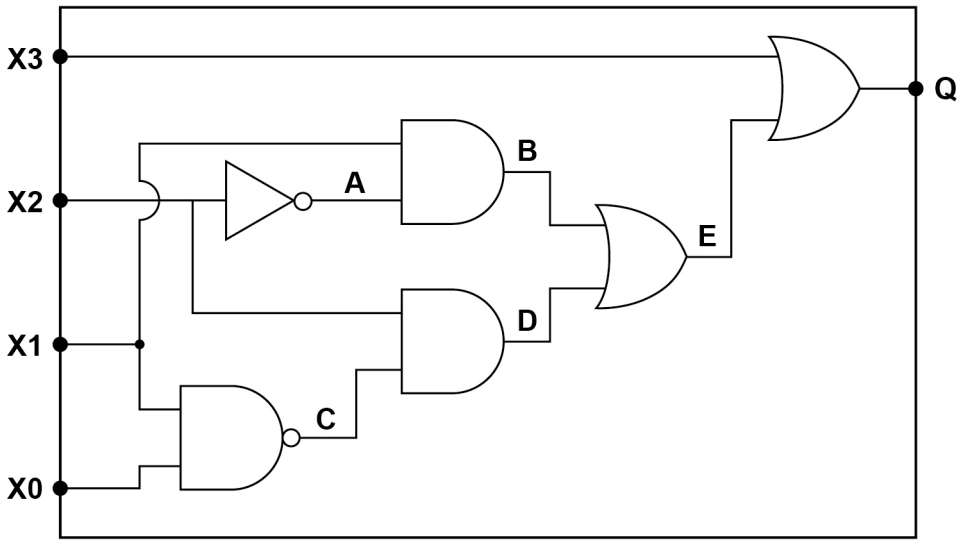


Figure 7 shows part of a logic circuit which is designed to take a binary representation of a single decimal digit as its input and light up the segments to display the decimal digit. The part of the circuit shown controls the lighting of **just one segment** of the display.

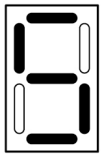
Figure 7



The inputs to the circuit are **X3**, **X2**, **X1** and **X0**. Together these form the binary representation of the decimal digit to display. For example, if the inputs to the circuit were:

X3	X2	X1	X0
0	1	0	1

then the display would need to show this pattern:



as 0101 is the binary representation of the decimal digit 5

The output **Q** is connected to one segment of the display. When **Q** is 1 this segment lights up, when it is 0 the segment does not light up.

0 8 . 2 Complete every empty cell in the truth table below for the circuit in **Figure 7**

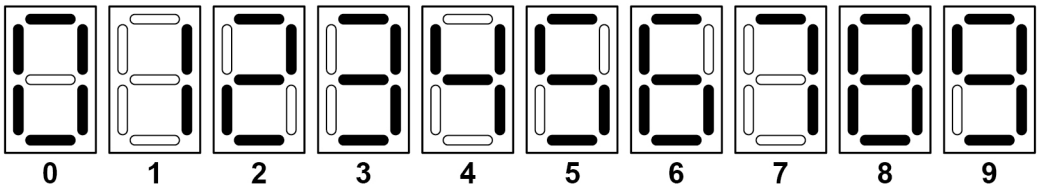
- The listed inputs to the table (**X3**, **X2**, **X1**, **X0**) represent the decimal digits 0–9 in binary, which are the only allowed inputs.
- The letters **A**–**E** have been used to label intermediate points on the circuit in **Figure 7** to help you to work out the final output **Q**
- Some of the cells have been completed for you.

[4 marks]

INPUTS				INTERMEDIATE POINTS					OUTPUT
X3	X2	X1	X0	A	B	C	D	E	Q
0	0	0	0						
0	0	0	1	1	0	1	0	0	0
0	0	1	0						
0	0	1	1	1	1	0	0	1	1
0	1	0	0						
0	1	0	1	0	0	1	1	1	1
0	1	1	0	0	0	1	1	1	1
0	1	1	1						
1	0	0	0	1	0	1	0	0	1
1	0	0	1						

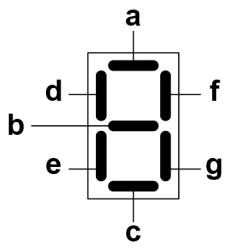
Figure 8 shows the patterns of segments that are illuminated for each of the decimal digits 0–9.

Figure 8



0 8 . 3 By considering the inputs and outputs of the circuit in **Figure 7** and consulting your trace table, state which of the segments in the display (labelled **a** to **g** below) the output **Q** from the circuit is controlling.

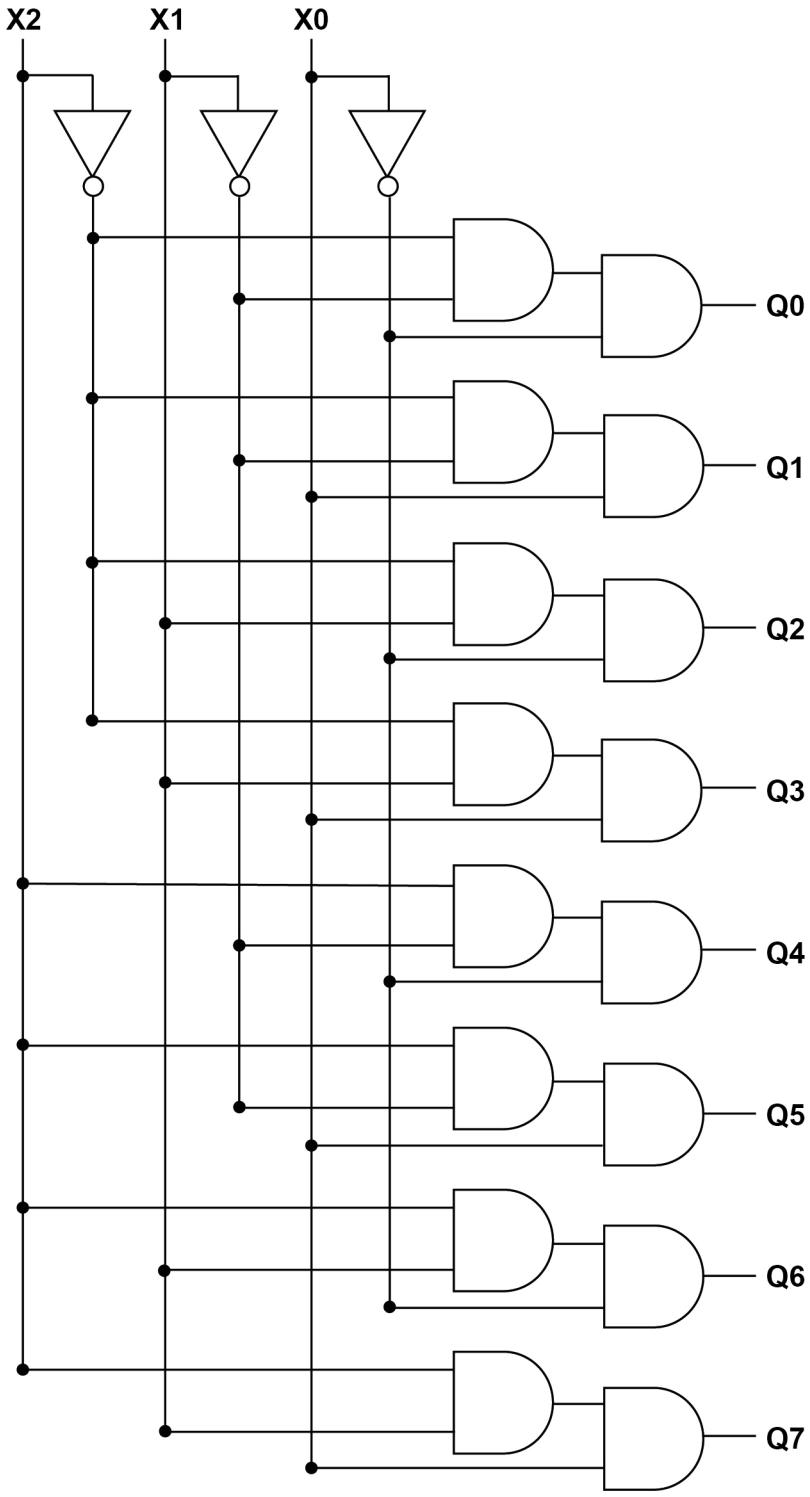
[1 mark]



Output **Q** is controlling segment _____

0 9 **Figure 1** shows a circuit with inputs **X0** to **X2** and outputs **Q0** to **Q7**

Figure 1



0 9 . 1 Write a Boolean expression to represent the output **Q1** of the circuit in **Figure 1**.

[1 mark]

Q1 = _____

0 9 . 2 Complete the truth table below for the circuit in **Figure 1**.

[3 marks]

INPUTS			OUTPUTS							
X2	**X1**	**X0**	**Q0**	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**
0	0	0								
0	0	1								
0	1	0								
0	1	1								
1	0	0								
1	0	1								
1	1	0								
1	1	1								

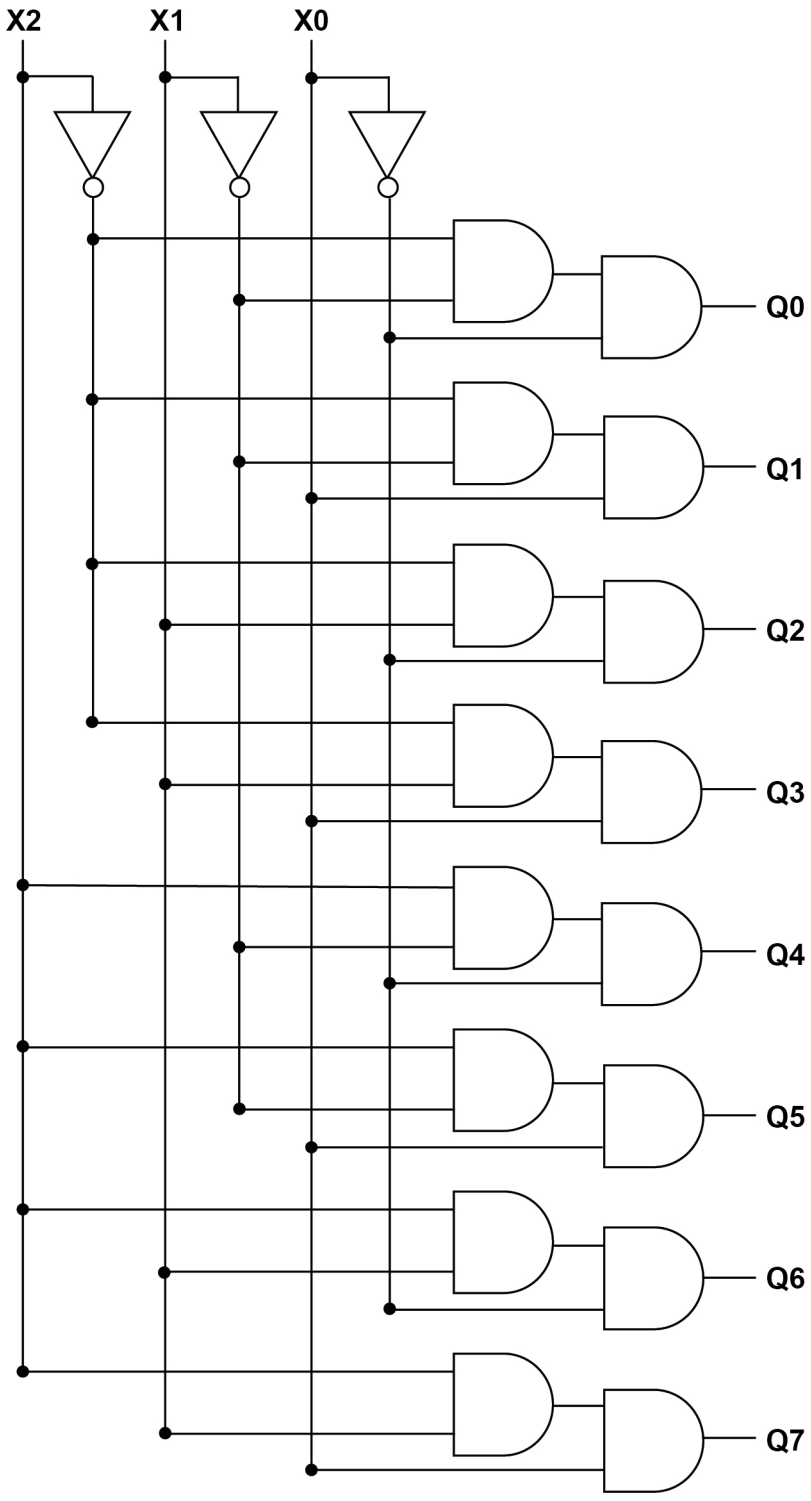
0 9 . 3 Explain the purpose of the circuit in **Figure 1**.

Considering the inputs and outputs of the circuit and consulting your answers to Question **04.1** and Question **04.2** may help you to do this.

[2 marks]

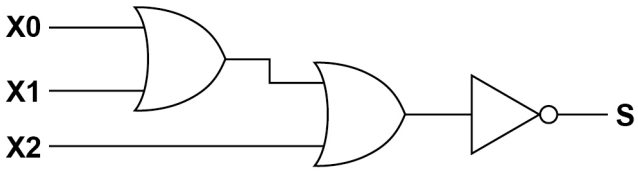
Figure 1 is repeated below to help you answer Question **04.4**.

Figure 1 (repeated)



0 9 . 4 The logic circuit in **Figure 2** produces an output **S** that is equivalent to one of the outputs of the logic circuit in **Figure 1**, for the inputs **X0**, **X1** and **X2**.

Figure 2



Which output (**Q0** to **Q7**) from **Figure 1** is the output **S** from the circuit in **Figure 2** equivalent to?

[1 mark]

1 0 . 1 Complete the truth table in **Figure 1** for the inputs A and B.

[1 mark]

Figure 1

A	B	$A + B$	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot \overline{B}$	$\overline{\overline{A} \cdot \overline{B}}$
0	0					
0	1					
1	0					
1	1					

1 0 . 2 The truth table in **Figure 1** demonstrates the correctness of an important law in Boolean algebra.

State the name of the law.

[1 mark]

1 1 The truth table in **Table 4** represents the operation of a logic system.

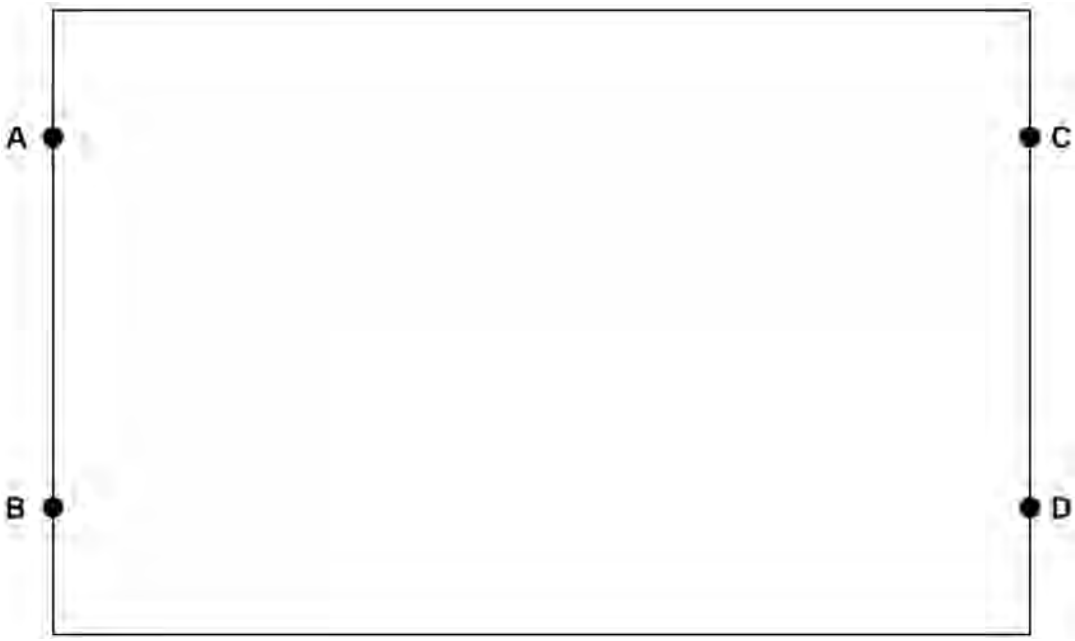
Table 4

Inputs		Outputs	
A	**B**	**C**	**D**
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

1 1 . 1 In the space below, draw a logic circuit that would produce the outputs shown in **Table 4** for the given inputs.

To achieve full marks for your response, your circuit should use **exactly two gates**.

[3 marks]



1 1 . 2 Explain the purpose of the circuit that you have drawn that produces the outputs given in **Table 4**.

[1 mark]

1 2 . 1 Draw a logic circuit for the Boolean expression:

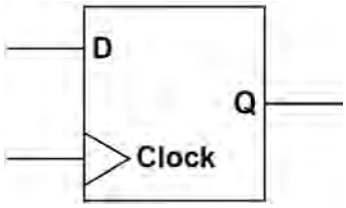
$$Q = \overline{\overline{A} \cdot B + \overline{B + C \cdot D}}$$

Do **not** simplify the expression.

[4 marks]

1 2 . 2 A flip-flop is a component that can be incorporated into a logic circuit. **Figure 3** shows a diagram of an edge-triggered D-type flip-flop.

Figure 3



Explain how the output **Q** will be affected when a pulse is received on the **Clock** input.

[1 mark]

1 2 . 3 Using the rules of Boolean algebra, simplify the following Boolean expression.

$$\overline{A} \cdot \left(B \cdot C \cdot D + B \cdot C \cdot \overline{D} + B \right) + \overline{\overline{A} + B}$$

You **must** show your working.

[4 marks]

Working

Answer